SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR
(AUTONOMOUS)
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : Electronic Devices (18EC0401) **Course & Branch**: B.Tech - ECE

Year & Sem: II-B.Tech & I-Sem **Regulation:** R18

UNIT –I

PN JUNCTION DIODE

I. Two Mark Questions:

1. What is depletion region? [L1][CO1][2M]
2. Define barrier potential. [L1][CO1][2M]
3. Why the resistance is decreased during forward bias? [L2][CO1][2M]
4. Define Breakdown Voltage of a PN junction diode. [L1][CO1][2M]
5. What do you understand by reverse saturation current? [L2][CO1][2M]
6. Write down the diode current equation. [L2][CO1][2M]
7. When a reverse bias is applied to a germanium PN junction diode, the reverse Saturation current at room temperature is 0.3μA. Determine the current flowing in the diode when 0.15V forward bias is applied at room temperature. [L3][CO1][2M]
8. Mention the types of Diode Capacitances. [L1][CO1][2M]
9. Define storage time and transition time of a PN junction diode. [L1][CO1][2M]
10. Mention the applications of PN Junction diode. [L1][CO1][2M]

II. Part – B Questions:

1. a) What is a PN Junction? Explain the formation of depletion layer in a PN junction. [L2][CO1][5M]
   b) Discuss the differences between Ideal Diode and Practical Diode. [L2][CO1][5M]
2. With neat diagrams, explain forward and reverse biasing of a PN Junction diode. Draw its V-I Characteristics. [L2][CO1][10M]
3. Derive the expression for depletion width of a PN Junction. [L2][CO1][10M]
4. Describe the energy band structure of open circuited PN Junction and derive the expression for Contact difference of potential. [L2][CO1][10M]
5. a) Derive the Diode Current Equation. [L1][CO1][5M]
   b) Write notes on Diode Resistance. [L2][CO1][5M]
6. a) What is transition capacitance? [L1][CO1][2M]
   b) Derive the expression for transition capacitance of a PN Junction Diode. [L3][CO1][8M]
7. a) Mention the importance of Diffusion capacitance. [L1][CO1][2M]
   b) Derive the expression for Diffusion capacitance of a PN Junction Diode. [L3][CO1][8M]
8. a) Describe the Temperature Dependence of PN Junction Diode on VI Characteristics. [L1][CO1][7M]
   b) Determine the value of forward current in the case of a PN junction diode, with I_o = 10μA, V_f = 0.8V at T = 300^0K. Assume Silicon Diode. [L3][CO1][3M]
9. a) Write notes on Breakdown in PN Junction diodes. [L2][CO1][5M]
   b) Find the factor by which the reverse saturation current of a silicon diode will get multiplied when the temperature is increased from 27^0C to 82^0C. [L3][CO1][5M]
10. Discuss about the switching characteristics of PN junction diode with suitable diagrams. [L2][C01][10M]
11. a) Mention the importance of Diode Clipper. Discuss the Positive and Negative Diode Clippers. [L1][CO1][5M]
    b) What is Clamper circuit? Describe about positive and negative clampers with neat circuit diagrams. [L1][CO1][5M]

UNIT –II

RECTIFIERS, FILTERS AND SPECIAL PURPOSE DEVICES

I. Two Mark Questions:

1. What is rectifier? [L1][CO2][2M]
2. Compare Half wave rectifier and Full wave rectifier. [L2][CO2][2M]
3. Define Peak Inverse Voltage of Half Wave Rectifier. [L1][CO2][2M]
4. What are the disadvantages of Half wave rectifier? [L2][CO2][2M]
5. Mention the advantages of Full Wave Rectifier. [L1][CO2][2M]
6. Write down the need for filters in power supplies. [L2][CO2][2M]
7. Calculate the ripple factor of a LC filter with FWR for a inductance of 10H and capacitance of 8μ for 50Hz AC input supply. [L3][CO2][2M]
8. What are the applications of Zener Diode? [L1][CO2][2M]
9. Mention the applications of Varactor Diode. [L1][CO2][2M]
10. Define Tunneling. [L1][CO2][2M]

II. Part – B Questions:

1. a) Draw the circuit diagram of half wave rectifier and explain its operation with the help Of waveforms. [L2][CO2][5M]
   b) Derive the expressions for Ripple Factor and Efficiency of Half Wave Rectifier. [L1][CO2][5M]
2. Derive the expressions for Average DC current, Average DC Voltage, RMS Value of Current, DC Power Output and AC Power Input of a Half Wave Rectifier. [L1][CO2][10M]
3. a) Draw the circuit diagram of Full wave rectifier and explain its operation with the help Of waveforms. [L2][CO2][5M]
   b) Derive the expressions for Ripple Factor and Efficiency of Full Wave Rectifier. [L1][CO2][5M]
4. Derive the expressions for Average DC current, Average DC Voltage, RMS Value of Current, DC Power Output and AC Power Input of a Full Wave Rectifier. [L1][CO2][10M]
5. A Half wave rectifier has a load of 3.5kΩ. If the diode resistance and the secondary coil Resistance together have resistance of 800Ω and the input voltage of 240V, Calculate (i) Peak, Average and RMS value of the current flowing, (ii) DC power output, (iii) AC Power input and (iv) efficiency of the rectifier. [L1][CO2][10M]
6. a) With neat diagram, explain Bridge Rectifier. [L2][CO2][5M]
   b) Compare the different types of filter circuits in terms of ripple factors. [L4][CO2][5M]
7. a) Explain the working of capacitor filter and derive the expression for ripple factor of Capacitor filter. [L3][CO2][5M]
   b) Derive the expression for ripple factor of inductor filter. [L3][CO2][5M]
8. a) Derive the Ripple Factor For L Section Filter. [L1][CO2][5M]
   b) Derive the expression for Ripple Factor of CLC Filter. [L1][CO2][5M]
9. a) Draw and discuss the VI characteristics of a Zener Diode. [L2][CO2][5M]
   b) Discuss about Varactor diode. [L1][CO2][5M]
10. a) Draw and describe VI characteristics of Tunnel Diode. [L2][CO2][5M]
    b) Describe the characteristics and applications of a photodiode. [L1][CO2][5M]
11. a) Explain the construction and applications of Solar Cell. [L2][CO2][5M]
    b) Draw and explain the basic structure of LED. Mention the applications of LED. [L2][CO2][5M]

UNIT –III

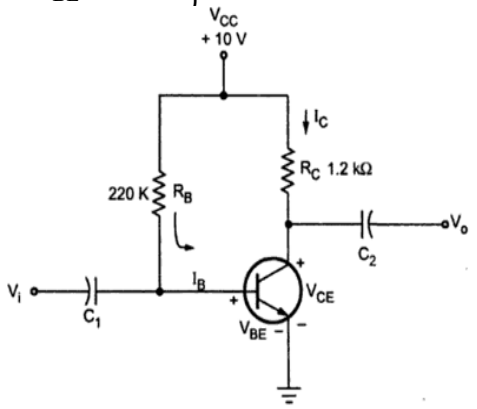
BIPOLAR JUNCTION TRANSISTOR

I. Two Mark Questions:

1. What are the different configurations of BJT? [L1][CO3][2M]
2. Mention the applications of Transistor. [L2][CO3][2M]
3. What do you mean by Punch Through Effect? [L1][CO3][2M]
4. Mention the three regions of operation of BJT. [L1][CO3][2M]
5. In Common Base connection, the emitter current is 6.28mA and the collector Current is 6.20mA. Determine common base current gain. [L3][CO3][2M]
6. If a transistor has $\alpha = 0.97$, find the value of β. [L3][CO3][2M]
7. Define Q Point of BJT. [L1][CO3][2M]
8. What is stability factor? [L1][CO3][2M]
9. Mention the disadvantages of fixed bias circuit of BJT. [L1][CO3][2M]
10. What is thermal runaway? How can it be avoided? [L2][CO3][2M]

II. Part – B Questions:

1. a) Discuss the operation of NPN transistor with diagram. [L2][CO3][5M]
   b) If the base current in a transistor is 20μA when the emitter current is 6.4mA, what are the values of α and β? Also calculate the collector current. [L3][CO3][5M]
2. a) What is early effect of a BJT? [L1][CO3][2M]
   b) With neat diagram, explain the Input and Output characteristics of a BJT in CB Configuration. [L2][CO3][8M]
3. Discuss the Input and Output characteristics of a BJT in CE Configuration. Indicate the regions of operations in the output characteristics. [L2][CO3][10M]
4. a) Describe the Input and Output characteristics of BJT in CC Configuration. [L2][CO3][5M]
   b) Write notes on Breakdown in transistors. [L1][CO3][5M]
5. a) Define Transistor Biasing and explain the need for Biasing? [L1][CO3][5M]
   b) Explain the concept of DC and AC Load lines and discuss the criteria for fixing the Q-point. [L2][CO3][5M]
6. a) Mention different types of Biasing a Transistor and explain the Fixed Bias of a Transistor [L2][CO3][5M]
   b) Explain Collector to Base bias of a Transistor with neat circuit diagram [L2][CO3][5M]
7. Derive the stability factors S, S' and S'' of a Transistor Voltage Divider bias. [L3][CO3][10M]
8. a) For the circuit shown in the Figure, calculate I_B, I_C, V_{CE}, V_B , V_C and V_{BC}. Assume that $V_{BE} = 0$ and $\beta = 50$. [L3][CO3][5M]



   b) Discuss Diode Compensation Technique for the parameters V_{BE} and I_{CO}. [L2][CO3][5M]
9. a) Describe Thermistor and Sensistor Compensation Techniques. [L1][CO3][5M]
   b) Discuss about Thermal Runaway and Thermal Resistance. [L2][CO3][5M]
10. Derive the condition for Thermal Stability to avoid thermal runaway. [L3][CO3][10M]
11. a) Derive the expression for Stability Factor S of a Fixed Bias Circuit. [L3][CO3][5M]
    b) Derive the expression for Stability Factor S of a Collector to Base Bias Circuit. [L3][CO3][5M]

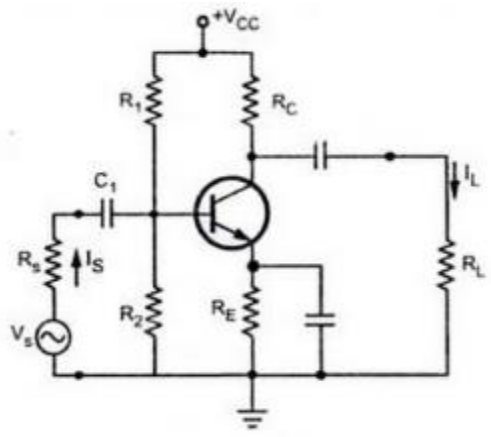
UNIT- IV
SMALL SIGNAL LOW FREQUENCY TRANSISTOR AMPLIFIER ANALYSIS

I. Two Mark Questions:

1. What are the salient features of hybrid parameters? [L1][CO4][2M]
2. Write the hybrid parameters conversion formulae for CC configuration in terms of CE configuration. [L2][CO4][2M]
3. Mention the hybrid parameters conversion formulae for CB configuration in terms of CE configuration.
4. Draw the generalized hybrid model for BJT amplifier. [L2][CO4][2M]
5. Write the expression for current gain A_I for common emitter transistor. [L2][CO4][2M]
6. Write the expression for output admittance Y_o for common emitter transistor. [L2][CO4][2M]
7. For a CE amplifier, if $h_{fe} = 50$, $h_{oe} = 25 \times 10^{-6}$ with load resistance of $R_L = 1k\Omega$, Calculate current gain A_I. [L3][CO4][2M]
8. Draw the approximate CE hybrid model of BJT. [L2][CO4][2M]
9. Draw the simplified hybrid model for CC amplifier. [L2][CO4][2M]
10. Draw the circuit diagram for single stage RC coupled amplifier using BJT. [L2][CO4][2M]

II. Part – B Questions:

1. a) Why hybrid model is used for the analysis of BJT amplifier at low frequencies? Draw the hybrid model for CE transistor and derive the parameters. [L2][CO4][5M]
   b) Compare the CE, CB and CC transistor amplifier parameters. [L2][CO4][5M]
2. Using low frequency h-parameter model, derive the expressions for voltage gain, current gain, input impedance and output admittance for a BJT Amplifier in CE configuration. [L3][CO4][10M]
3. a) With neat diagram, derive the CE amplifier parameters using approximate analysis. [L2][CO4][5M]
   b) Obtain the expressions for current gain, voltage gain, input impedance and output impedance of CB amplifier using simplified hybrid model. [L2][CO4][5M]
4. a) Determine the parameters A_I, R_i, A_v and R_0 of Emitter Follower using simplified hybrid model analysis. [L3][CO4][5M]
   b) A voltage source of internal resistance $R_s = 900\Omega$ drives a CC amplifier using load resistance $R_L=2000\Omega$. The CE h parameters are $h_{fe}=60$, $h_{ie}=1200\Omega$, $h_{oe} = 25\mu A/V$ and $h_{re} = 2 \times 10^{-4}$. Compute A_I, R_i, A_v and R_0 using approximate analysis. [L3][CO4][5M]
5. A CE amplifier is driven by a voltage source of internal resistance $R_s = 800\Omega$ and the load impedance of $R_L=1000\Omega$. The h-parameters are $h_{ie}=1k$, $h_{fe}=50$, $h_{oe} = 25\mu A/V$ and $h_{re} = 2 \times 10^{-4}$. Calculate current gain, voltage gain, input impedance and output impedance using exact analysis and approximate analysis. [L3][CO4][10M]
6. For a CB transistor amplifier driven by a voltage source of internal resistance $R_s = 1200\Omega$, the load Impedance of $R_L = 1000\Omega$. The h parameters are $h_{ib} = 22\Omega$, $h_{rb} = 3 \times 10^{-4}$, $h_{fb} = -0.98$, $h_{ob} = 0.5\mu A/V$. Calculate current gain, voltage gain, input impedance and output impedance using exact analysis and approximate analysis. [L3][CO4][10M]
7. Consider a single stage CE amplifier with $R_s = 1k\Omega$, $R_1 = 50k\Omega$, $R_2 = 2k\Omega$, $R_c = 1k\Omega$, $R_L = 1.2k\Omega$, $h_{fe}=50$, $h_{ie}=1.1k$, $h_{oe} = 25\mu A/V$ and $h_{re} = 2.5 \times 10^{-4}$, as shown in Fig. Find A_I, R_i, A_v, A_{vs}, A_{IS} and R_0. [L3][CO4][10M]



8. a) Obtain the expression for current gain, voltage gain, input impedance and output impedance For Common Emitter Amplifier with Emitter Resistor. [L2][CO4][5M]

b) A CE amplifier is driven by a voltage source of internal resistance $R_s = 1000\Omega$ and the load impedance of $R_C=2k\Omega$. The h-parameters are $h_{ie}=1.3k$, $h_{fe}=55$, $h_{oe} = 22\mu A/V$ and $h_{re} = 2 \times 10^{-4}$. Neglecting biasing resistors, compute current gain, voltage gain, input impedance, output impedance for the value of Emitter Resistor $R_E = 200\Omega$ inserted in the emitter circuit. [L3][CO4][5M]

9. a) Draw the circuit diagram of a single stage RC coupled Amplifier and discuss the steps used for designing it. [L2][CO4][5M]

b) Determine Voltage Gain, Current Gain, Input resistance and Output resistance for a CE amplifier using NPN transistor with $h_{ie} = 1200\Omega$, $h_{re} = 0$, $h_{fe} = 36$ and $h_{oe} = 2 \times 10^{-6}$ mhos, $R_L = 2.5k\Omega$ and $R_S = 500\Omega$ (neglect the effect of biasing circuit). [L3][CO4][5M]

10. Design a single stage RC coupled BJT amplifier for the following values. Assume that for Silicon transistor, $V_{cc} = 10V$, $I_c = 4mA$, $h_{fe} = 100$, $h_{ie} = 1k\Omega$, $R_{L-} = 100k\Omega$ and $f_L = 100Hz$. [L3][CO4][10M]

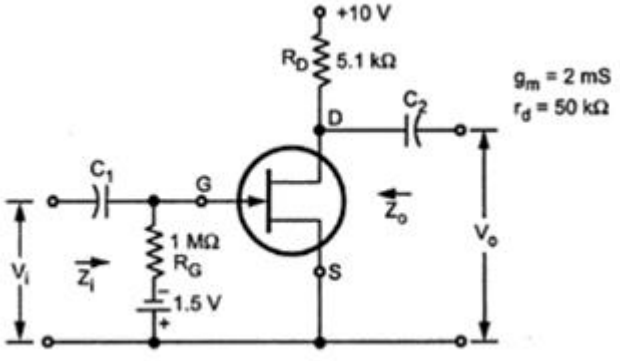
UNIT- V
FIELD EFFECT TRANSISTOR

I. Two Mark Questions:

1. Why a Field Effect Transistor is called so? [L1][CO5][2M]
2. Mention the advantages of FET? [L2][CO5][2M]
3. Define Pinch off Voltage. [L1][CO5][2M]
4. Define drain resistance of JFET. [L1][CO5][2M]
5. What is transconductance of JFET. [L1][CO5][2M]
6. What is MOSFET? Classify the types of MOSFET. [L1][CO5][2M]
7. Draw the symbol for depletion and enhancement n channel MOSFET. [L2][CO5][2M]
8. Draw the drain characteristics of n-channel enhancement MOSFET. [L2][CO5][2M]
9. What is the need for oxidation process in IC fabrication. [L2][CO5][2M]
10. What do you mean by photolithography in IC fabrication process? [L1][CO5][2M]

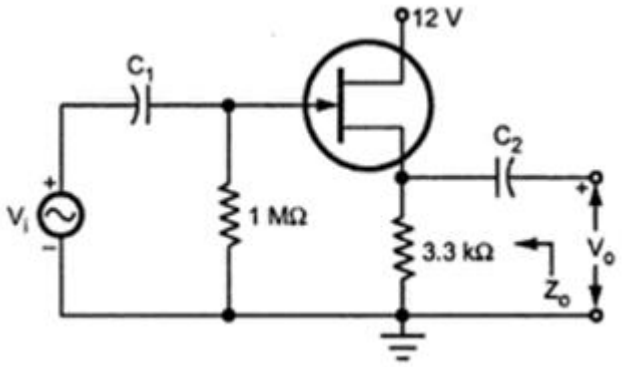
II. Part – B Questions:

1. a) Describe the construction and working principle of N-channel JFET. [L2][CO5][8M]
   b) Mention the applications of JFET. [L1][CO5][2M]
2. a) Define the JFET Volt-Ampere Characteristics and determine FET parameters. [L1][CO5][5M]
   b) Compare the performance of BJT with FET. [L3][CO5][5M]
3. a) With the help of neat diagram, explain the operation and characteristics of n-channel enhancement type MOSFET. [L2][CO5][8M]
   b) Mention the differences between depletion and enhancement MOSFET. [L3][CO5][2M]
4. Discuss the operation and characteristics of n-channel depletion type MOSFET with diagram. [L2][CO5][10M]
5. a) Draw and explain the small signal model of FET at low frequency. [L1][CO5][4M]
   b) For the circuit shown in Fig. determine input impedance, output impedance and voltage gain. [L4][CO5][6M]



6. Derive input impedance, output impedance and voltage gain of JFET Common Drain amplifier with neat diagram. [L2][CO5][10M]

7. a) Discuss JFET Fixed Bias with neat diagram and derive the expression for Input impedance, Output impedance and Voltage gain. [L3][CO5][8M]
   b) Compare n channel JFET with p channel JFET. [L3][CO5][2M]
8. a) Draw the circuit diagram of JFET Common Source amplifier with voltage divider bias for bypassed R_s and determine the expression for input impedance, output impedance and voltage gain. [L2][CO5][5M]
   b) For Common Drain Amplifier as shown in the Figure, g_m = 2.5mS, r_d = 25KΩ. Calculate Input impedance, Output impedance and Voltage gain. [L4][CO5][5M]



9. List and explain the steps involved in the manufacturing process of monolithic ICs. [L2][CO5][10M]
10. Discuss CMOS fabrication process with neat diagram. [L1][CO5][10M]

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UNIT –I
PN JUNCTION DIODE

1. The static resistance of a diode is [ ]
   A) its opposition to the DC current flow B) its opposition to the AC current flow
   C) resistance of diode when forward biased D) none of the above
2. When the reverse bias is applied to a junction diode, it [**GATE 2015]** [ ]
   A) lowers the potential barrier B) raises the potential barrier
   C) greatly decreases the minority carrier current D) greatly increases the minority carrier current
3. Doping of semiconductor is [ ]
   A) the process of purifying semiconductor materials
   B) the process of adding certain impurities to the semiconductor material in controlled amounts
   C) the process of converting semiconductor material into some form of active device such as FET
   D) one of the steps used in the fabrication of ICs
4. Referring to the energy level diagram of semiconductor materials, the width of forbidden energy gap is about **[GATE 2003]** [ ]
   A) 10eV B) 100eV C) 1eV D) 0.1eV
5. A PN junction diode **[IES 2014]** [ ]
   A) has high resistance in both forward and reverse directions
   B) has low resistance in the forward direction
   C) has high resistance in the forward direction
   D) has low resistance in the reverse direction
6. If a PN junction is not biased, the junction current at equilibrium is [ ]
   A) zero as no charges cross the junction
   B) zero as equal number of carriers cross the barrier
   C) mainly due to diffusion of majority charge carriers
   D) mainly due to top diffusion of majority charge carriers
7. In a PN junction, the potential barrier is due to the charges on either side of the junction, which consists of [ ]
   A) fixed donor and acceptor ions B) majority carriers only
   C) minority carriers only D) both majority and minority carriers
8. In a PN junction, the region containing the uncompressed acceptor and donor ions is called **[GATE 2007]** [ ]
   A) transition zone B) depletion region C) neutral region D) active region
9. In a forward biased PN junction diode, the [ ]
   A) positive terminal of the battery is connected to the P side and the negative to the N side
   B) positive terminal of the battery is connected to the N side and the negative to the P side
   C) junction is earthed
   D) none of the above
10. When PN junction is forward biased [ ]
    A) electrons in the N region are injected into the P region
    B) holes in the P region are injected into the N region
    C) both (a) and (b)
    D) None of the above
11. When we apply reverse bias to a junction diode, it [ ]
    A) lowers the potential barrier B) raises the potential barrier
    C) greatly decreases the minority carrier current D) greatly increases the majority carrier current
12. Under normal operating voltage, the reverse current in a silicon diode is about [ ]

A) 10mA B) 1μA C) 1000 μA D) None of the above

13. The increased depletion region in a PN diode is due to **[GATE 2015]** [ ]
A) reverse biasing B) forward biasing
C) an area created by crystal doping D) an area void of current carriers

14. When a diode is forward biased, [ ]
A) barrier potential increases B) barrier potential decreases
C) majority current decreases D) minority current decreases

15. For a Germanium PN junction, the maximum value of barrier potential is **[IES 2009]** [ ]
A) 0.3V B) 0.7V C) 1.3V D) 1.7V

16. For a Silicon PN junction, the maximum value of barrier potential is **[GATE 2015]** [ ]
A) 0.3V B) 0.7V C) 1.3V D) 1.7V

17. When holes leave the p material to fill electrons in the n material, the process is called [ ]
A) mixing B) depletion C) diffusion D) none of the above

18. The decreased depletion region in a PN junction is due to [ ]
A) reverse biasing B) forward biasing
C) diffusion D) none of the above

19. Current flow in a semiconductor depends on the phenomenon [ ]
A) drift B) diffusion C) recombination D) All of the above

20. In a semiconductor diode, V – I relationship is such that [ ]
A) current varies linearly with voltage B) current increases exponentially with voltage
C) current varies inversely with voltage D) none of these

21. The capacitance appearing across a reverse biased semiconductor junction **[GATE 2001]** [ ]
A) increases with increase in bias voltage B) decreases with increase in bias voltage
C) is independent of bias voltage D) none of these

22. The PN junction diode is a [ ]
A) passive device B) vacuum tube C) unilateral device D) bilateral device

23. A certain amount of diode current still flows when diode is under reverse bias condition. What is this current called? [ ]
A) Reverse bias current B) Reverse saturation current
C) Reverse diode Current D) Diode off current

24. The number of minority carriers crossing the junction of a PN junction diode depends Primarily on **[GATE 2013]** [ ]
A) concentration of doping impurities B) magnitude of potential barrier
C) magnitude of forward bias voltage D) rate of thermal generation of electron hole pairs

25. Reverse saturation current in a germanium diode is of the order of [ ]
A) 1nA B) 1μA C) 1mA D) 10mA

26. The diffusion capacitance of a forward biased PN junction diode with a steady current I depends on **(GATE 1987)** [ ]
A) width of the depletion region B) mean lifetime of holes
C) mean lifetime of electrons D) junction area

27. Zener breakdown occurs [ ]
A) due to normally generated carriers B) in lightly doped junctions
C) due to rupture of covalent bonds D) mostly in germanium junctions

28. A breakdown which is caused by cumulative multiplication of carriers through field induced Impact ionization occurs in **(GATE 2015)** [ ]
A) Zener diode B) Tunnel Diode
C) Varactor Diode D) Avalanche Diode

29. For a highly doped diode **(GATE 1989)** [ ]
A) Zener breakdown is like to take place B) Avalanche breakdown is like to take place
C) either (a) or (b) will take place D) neither (a) or (b) will take place

30. The breakdown that occurs in the reverse biased condition in a narrow junction diode is [ ]
A) Zener Breakdown B) Avalanche Breakdown C) both (a) and (b) D) None

31. The breakdown that occurs in the reverse biased condition in a wider junction diode is [ ]
A) Zener Breakdown B) Avalanche Breakdown C) both (a) and (b) D) None

32. The Volt Equivalent Temperature V_T for a room temperature is **[GATE 2010]** [ ]
A) 20V B) 1mV C) 26mV D) none of the above

33. Practically, the value of dV/dT is assumed to be _____ for either Ge or Si at room Temperature. [ ]
A) -2.5mV/^{0}C B) -4.7mV/^{0}C C) -26mV/^{0}C D) none of the above
34. The reverse saturation current I_0 increases by _____ change in temperature for both Si and Ge Diodes. [ ]
A) 10% per ^{0}C B) 7% per ^{0}C C) 2.3% per ^{0}C D) 20% per ^{0}C
35. The reverse saturation current approximately doubles for every _____ rise in temperature. [ ]
A) 30^{0}C B) 20^{0}C C) 10^{0}C D) none of the above
36. The circuit with which the waveform is shaped by removing a portion of the input signal Without distorting the remaining part of AC signal is called [ ]
A) Clamper B) Multivibrator C) Clipper D) None of the above
37. Clipping circuits are also called as [ ]
A) Voltage or Current limiter B) Amplitude Selector C) Slicers D) All of the above
38. If a small portion of positive or negative half cycle of the signal voltage is to be removed, then the type of clipper used is [ ]
A) Biased Clipper B) Positive Clipper C) Negative Clipper D) none of the above
39. A circuit which introduces a DC level to an AC signal is called [ ]
A) Clipper B) Clamper C) Tuned Amplifier D) Blocking Oscillator
40. A dc restorer is a [ ]
A) Clipper B) Tuned Amplifier C) Clamper D) Blocking Oscillator

UNIT –II
RECTIFIERS, FILTERS & SPECIAL PURPOSE DEVICES

1. A rectifier is used to [ ]
A) convert AC voltage to DC Voltage B) convert DC voltage to AC Voltage
C) both (a) and (b) D) convert voltage to current
2. The ripple factor of a Half Wave Rectifier is [ ]
A) 1.21 B) 0.482 C) 0.406 D) 0.121
3. The peak inverse voltage of a Half Wave Rectifier is [ ]
A) V_m B) 2 V_m C) $V_m/2$ D) 3V_m
4. The efficiency of a Half Wave Rectifier is [ ]
A) 40.6% B) 81.2% C) 1.12% D) 48.2%
5. The ripple factor of Full wave rectifier is **[IES 2012]** [ ]
A) 1.21 B) 0.482 C) 0.406 D) 0.121
6. The peak inverse voltage of a full Wave Rectifier is [**GATE 2004]** [ ]
A) V_m B) 2 V_m C) $V_m/2$ D) 3V_m
7. The efficiency of a full Wave Rectifier is [ ]
A) 40.6% B) 81.2% C) 1.12% D) 48.2%
8. The peak inverse voltage of a Bridge Rectifier is [ ]
A) V_m B) 2 V_m C) $V_m/2$ D) 3V_m
9. The bridge rectifier requires [**GATE 2001]** [ ]
A) 2 diodes B) 3 diodes C) 4 diodes D) 8 diodes
10. The primary function of a rectifier filter is to [ ]
A) suppress old harmonics B) remove ripples
C) Stabilize the output dc level D) minimize the input ac variations
11. The theoretical maximum efficiency of a Full wave circuit is [ ]
A) the same as that os Half wave circuit B) Double as that of a half wave circuit
C) definitely more but less than double that of a half wave circuit D) none of these
12. In a full wave rectifier circuit, the peak inverse voltage per diode is [ ]
A) the same as that is a half wave rectifier circuit B) half the value in half wave rectifier circuit
C) double the value in half wave rectifier circuit D) none of these
13. In a half wave rectifier circuit, the load current flows **[GATE 1997]** [ ]
A) only for the positive half cycle of the input signal
B) for less than half cycle of the input signal
C) for more than half cycle of the input signal
D) for whole cycle of the input signal

14. In a full wave bridge rectifier, if V_m is the PIV across the secondary of the transformer, the maximum voltage coming across each reverse biased diode is [ ]
A) V_m B) $2\ V_m$ C) $V_m/2$ D) None of these
15. In capacitor filter, the ripple factor decreases with [**GATE 2011]** [ ]
A) decrease in C B) increase in C
C) increase in frequency D) decrease in frequency
16. The diode used in voltage regulator is [ ]
A) PN junction diode B) Varactor Diode C) Zener Diode D) GUNN diode
17. The ripple factor of a inductor filter is [ ]
A) $R_L w/(\sqrt{2}\sqrt{3}L)$ B) $R_L/(\sqrt{2}\sqrt{3}L)$ C) $R_L/(3\sqrt{2}wL)$ D) $R_L/(2\sqrt{3}wL)$
18. A half wave rectifier is equivalent to [**GATE 2006]** [ ]
A) a clamper circuit B) a clipper circuit
C) a clamper circuit with negative bias D) a clamper circuit with positive bias
19. The basic reason why a full wave rectifier has a twice the efficiency of a half wave rectifier is that :[**GATE 1997]** [ ]
A) it makes use of transformer B) its ripple factor is much less
C) it utilizes both half cycle of the input D) its output frequency is double the line frequency
20. The DC power output for HWR is [ ]
A) $(I_m^2/\pi^2)R_L$ B) $I_m/2$ C) $(I_m/2)\ R_L$ D) $I_m.R_L$
21. The TUF for Bridge Rectifier is [ ]
A) 0.287 B) 0.693 C) 0.812 D) 0.963
22. The amount of ac content in the output can be mathematically expressed by a factor called [ ]
A) TUF B) Ripple factor C) PIV D) PRV
23. The TUF for HWR is [**BSNL(TTA) 2015]** [ ]
A) 1.211 B) 0.86 C) 0.287 D) 0.911
24. Zener diode is usually operated **[GATE 1989]** [ ]
A) in forward bias mode B) in reverse bias mode
C) near cut in voltage D) in forward linear region
25. Which one of the following diode is used for voltage stabilization? [**GATE 2011]** [ ]
A) PN Junction B) Tunnel C) Varactor D) Zener
26. Which of the following statement is best suited for a Zener diode? [ ]
A) It is rectifier diode B) It works in the forward biased region
C) It is a constant voltage device D) It is mostly used in clipping circuit
27. A tunnel diode [ ]
A) is a reverse recovery diode B) has heavy doping
C) is a power diode D) has light doping
28. Which one of the following diodes shows the negative resistance region? **[GATE 2002]** [ ]
A) PN Junction B) Tunnel C) Zener D) Varactor
29. The most important application of a Tunnel diode is [ ]
A) rectifier B) switching device C) voltage controlled device D) none of these
30. The VI characteristics of a Tunnel diode exhibit a [ ]
A) multiuvalued function of voltage B) multivalued function of current
C) single value function of current D) none of these
31. The main reason why electrons can tunnel through a PN junction is that **[GATE 2009]** [ ]
A) they have high energy B) barrier potential is very low
C) depletion layer is extremely thin D) impurity level is low
32. The I_p / I_v ratio of tunnel diode is of primary importance in [ ]
A) determining tunneling speed of electrons B) the design of an oscillator
C) amplifier designing D) computer applications
33. Silicon is preferred for manufacturing Zener diodes because [ ]
A) is relatively cheap B) needs lower doping level
C) has high temperature and current capacity D) has lower breakdown voltage
34. LEDs are fabricated from [ ]
A) silicon B) germanium C) Si or Ge D) gallium arsenide
35. A photodiode is used in reverse bias because [ ]
A) majority swept are reverse across the junction

B) only one side is illuminated
C) reverse current is small when compared to photocurrent
D) reverse current is large when compared to photocurrent

36. Which one of the following statement is correct? A photo diode works on the principle of **[GATE 1990]** [ ]
A) photovoltaic effect B) photoconductive effect
C) photoelectric effect D) photothermal effect

37. A LED is basically which one of the following biased PN Junction? [ ]
A) forward biased B) reverse biased C) lightly doped D) heavily doped

38. GaAs LEDs emit radiation in the **[GATE 1992]** [ ]
A) ultraviolet region B) violet blue green range of the visible region
C) visible region D) infra red region

39. A Varactor diode is also called as [ ]
A) Voltage variable capacitor B) TRIAC C) DIAC D) none of the above

40. Solar cell works under the principle of [ ]
A) Hall Effect B) piezo electric effect C) Photovoltaic Effect D) none of the above

UNIT III
BIPOLAR JUNCTION TRANSISTOR

1. A collector collects [ ]
A) electrons from the base in case of PNP transistors
B) electrons from the emitter in case of PNP transistors
C) holes from the base in case of NPN transistors
D) holes from the base in case of PNP transistors

2. In a PNP transistor with normal bias, **[GATE 2015]** [ ]
A) the collector junction has negligible resistance
B) only holes cross the collector junction
C) the CB junction is reverse biased and the EB junction is forward biased
D) only majority carriers cross the collector junction

3. A PNP transistor is made of **[GATE 2004]** [ ]
A) Silicon B) Germanium C) either silicon or Germanium D) none of the above

4. In most transistors, the collector region is made physically larger than the emitter Region [ ]
A) for dissipating heat
B) to distinguish it from others
C) as it is sensitive to ultraviolet rays
D) to reduce resistance in the path of flow of electrons

5. The three terminals of a BJT are called [ ]
A) PNP B) NPN C) anode, cathode and gate D) emitter, base and collector

6. For a NPN transistor, the N regions are [ ]
A) emitter and base B) base and collector C) emitter and collector D) None

7. For operation of PNP amplifier, the base of the amplifier must be [ ]
A) 0 V B) positive with respect to collector
C) negative with respect to collector D) greater than the collector current

8. In a transistor, the region that is very lightly doped and very thin is the [ ]
A) emitter B) base C) collector D) None of the above

9. In a NPN transistor, the emitter [ ]
A) emits or injects holes into the collector B) emits or injects electrons into the collector
C) emits or injects holes into the base D) emits or injects holes into the base

10. In a PNP transistor with normal bias, the emitter junction [ ]
A) is always reverse biased B) offers very high resistance
C) offers a low resistance D) remains open

11. In a NPN transistor, when the emitter junction is forward biased and the collector junction Is reverse biased, the transistor will operate in the [**GATE 1995]** [ ]
A) active region B) saturation region C) cutoff region D) None of the above

12. In a PNP transistor, electrons flow [ ]

A) into the transistor at the collector only
B) into the transistor at the base and the collector leads
C) out of the transistor at the base and the collector leads
D) out of the transistor at the base collector as well as emitter leads

13. The arrow head on a transistor symbol indicates [ ]
A) direction of electron current in the emitter B) direction of hole current in the emitter
C) diffusion current in the emitter D) drift current in the emitter

14. Power transistors are invariably provided with [ ]
A) soldered connections B) Heat Sink C) metallic casting D) None

15. The largest current flow of a bipolar transistor occurs [ ]
A) in emitter B) in base C) in collector D) through emitter-collector

16. Conventional biasing of a bipolar transistor has **[GATE 2007]** [ ]
A) EB forward biased and CB forward biased B) EB reverse biased and CB forward biased
C) EB forward biased and CB reverse biased D) EB reverse biased and CB reverse biased

17. The common emitter transistor circuit has [ ]
A) high gain B) low gain C) negligible gain D) zero gain

18. In an NPN transistor, if both the emitter junction and collector junction are reverse biased, then the transistor will operate in [ ]
A) active region B) saturation region C) cutoff region D) none of the above

19. In a normally biased NPN transistor, the main current crossing the collector junction is [ ]
A) a drift current B) a hole current C) a diffusion current D) same as base current

20. In a PNP transistor, the electrons flow into the transistor at the [ ]
A) collector only B) emitter only C) emitter and base D) collector and base

21. The forward current gain, h_{fe}, is defined as [ ]
A) V_{BE} / I_B, V_{CE} constant B) I_B / I_C, V_{CE} constant
C) I_C / I_B, V_{CE} constant D) I_C / I_B, V_{BE} constant

22. The α and β of a transistor are related to each other as [ ]
A) $\alpha = \beta / (1+\beta)$ B) $\beta = \alpha / (1+\alpha)$ C) $\beta = (1+\alpha) / \alpha$ D) $\alpha = (1+\beta) / \beta$

23. The transistor configuration which provides highest output impedance is [ ]
A) Common Base B) Common Emitter C) Common Collector D) None of the above

24. For $\alpha = 0.99$, the value of β is **[GATE 2007]** [ ]
A) 9.9 B) 49 C) 99 D) 100

25. The operating point variation is due to [ ]
A) I_{co} B) V_{BE} C) β D) All the above

26. Which of the following conditions ensures that the transistor does not undergo thermal runaway? [ ]
A) $V_{CE} = V_{CC} / 2$ B) $V_{CE} < V_{CC} / 2$ C) $V_{CE} < V_{CC}$ D) $V_{CE} > V_{CC} / 2$

27. The stability factor of a fixed bias is [ ]
A) $1 + \beta$ B) $1 - \beta$ C) $\beta / 1 - \beta$ D) $1 / 1 - \beta$

28. The leakage current in CE configuration may be around [**IES 2016]** [ ]
A) few nanoamperes B) few microamperes
C) few hundred microamperes D) few milliamperes

29. The quiescent point of a transistor biasing circuit implies [ ]
A) zero bias B) no output C) no distortion D) no input signal

30. For normal amplification, the Q-point should be established in the [ ]
A) active region B) saturation region C) cutoff region D) none of the above

31. The biasing technique which gives good stability is **[GATE 2015]** [ ]
A) Collector to base bias B) Fixed Bias C) Self Bias D) none of the above

32. Stability factor S is approximately unity for [ ]
A) Collector to base bias B) Fixed Bias C) Self Bias D) none of the above

33. Which of the following transistor parameters are functions of temperature: [ ]
A) β alone B) I_{CO} alone C) V_{BE} alone D) all of the above

34. The self bias arrangement gives an improved Q-point stability when [ ]
A) R_E is low B) β is small, but R_E is large C) both β and R_E are large D) none

35. The biasing method which is considered independent of transistor β is **[GATE 1990]** [ ]

A) fixed bias B) collector feedback bias C) voltage divider bias D) none

36. The biasing configuration that offers least stability is [ ]
A) fixed bias B) collector feedback bias C) voltage divider bias D) none

37. Which one of the following statements is correct? [**GATE 2011]** [ ]
A) Both I_{CO} and V_{BE} increase with temperature
B) Both I_{CO} and V_{BE} decrease with temperature
C) I_{CO} increases with temperature and V_{BE} decreases with temperature
D) I_{CO} decreases with temperature and V_{BE} increases with temperature

38. The collector current for the CE circuit is given $I_c = \beta I_B + (1 + \beta) I_{CO}$. The three variables β, I_B and I_{co} **[GATE 2013]** [ ]
A) increase with rise in temperature B) increase with fall in temperature
C) decrease with rise in temperature D)decrease with fall in temperature

39. The resistance of thermistor decreases exponentially with [ ]
A) increase of temperature B) decrease of temperature C) constant temperature D) none

40. The stability factor S is [ ]
A) dI_c / dI_{c0} B) dI_c / dV_{BE} C) $dI_c / d\beta$ D) none of the above

UNIT IV
SMALL SIGNAL LOW FREQUENCY TRANSISTOR AMPLIFIER ANALYSIS:

1. h parameters are also called as [ ]
A) admittance parameters B) hybrid parameters
C) impedance parameters D) reluctance parameters

2. The parameter h_{11} has the dimension of [ ]
A) Ω B) ℧ C) V D) dimensionless

3. The parameter h_{12} has the dimension of [ ]
A) Ω B) ℧ C) V D) dimensionless

4. The parameter h_{21} has the dimension of [ ]
A) Ω B) ℧ C) V D) dimensionless

5. The parameter h_{22} has the dimension of [ ]
A) Ω B) ℧ C) V D) dimensionless

6. The parameter h_i is called as [ ]
A) input impedance B) output admittance C) reverse voltage gain D) forward current gain

7. The parameter h_r is called as **[GATE 1995]** [ ]
A) input impedance B) output admittance C) reverse voltage gain D) forward current gain

8. The parameter h_f is called as [ ]
A) input impedance B) output admittance C) reverse voltage gain D) forward current gain

9. The parameter h_o is called as [ ]
A) input impedance B) output admittance C) reverse voltage gain D) forward current gain

10. The amplifier that gives unity voltage gain is **[GATE 2017]** [ ]
A) common emitter B) common collector C) common base D) common gate

11. The amplifier that gives maximum power gain is [**IES 2014]** [ ]
A) common emitter B) common collector C) common base D) common gate

12. The amplifier that gives 180^0 phase shift is [**IES 2011]** [ ]
A) common emitter B) common collector C) common base D) common gate

13. The common collector amplifier is also called as **[GATE 1994]** [ ]
A) collector follower B) base Follower C) emitter follower D) none of the above

14. The h parameters approach gives correct results for [ ]
A) Large Signals only B) Small Signals only C) Both large and small signals D) none

15. An emitter follower is used as [ ]
A) a power amplifier B) an impedance matching device
C) a low input impedance circuit D) a follower of base signal

16. The expression for current gain A_I for CE amplifier is [ ]
A) $-h_{fe} / (1 + h_{oe}R_L)$ B) A_iR_L / Z_i C) $h_{ic} + h_{rc} A_i R_L$ D) $h_{oe} - [(h_{fe}h_{re}) / (h_{ie} + R_s)]$

17. The expression for voltage gain A_V for CB amplifier is [ ]
A) $-h_{fe} / (1 + h_{oe}R_L)$ B) A_iR_L / Z_i C) $h_{ic} + h_{rc} A_i R_L$ D) $h_{oe} - [(h_{fe}h_{re}) / (h_{ie} + R_s)]$

18. The expression for input impedance Z_I for CC amplifier is [ ]

A) $-h_{fe} / (1 + h_{oe}R_L)$ B) A_iR_L / Z_i C) $h_{ic} + h_{rc} A_i R_L$ D) $h_{oe} - [(h_{fe}h_{re}) / (h_{ie} + R_s)]$

19. The expression for output admittance Y_o for CE amplifier is [ ]
A) $-h_{fe} / (1 + h_{oe}R_L)$ B) A_iR_L / Z_i C) $h_{ic} + h_{rc} A_i R_L$ D) $h_{oe} - [(h_{fe}h_{re}) / (h_{ie} + R_s)]$

20. The relation between A_{vs} and A_{is} is [ ]
A) $A_{vs} = A_{is} R_L / R_s$ B) $A_{vs} = A_{is}$ C) $A_{vs} = R_L / R_s A_{is}$ D) $A_{vs} = h_i h_o / A_{is}$

21. In simplified hybrid model of CE, the current gain is [ ]
A) $-h_{fe}$ B) $A_i R_L / h_{ie}$ C) h_{ie} D) infinity

22. In simplified hybrid model of CE, the voltage gain is [ ]
A) $-h_{fe}$ B) $A_i R_L / h_{ie}$ C) h_{ie} D) infinity

23. In simplified hybrid model of CE, the input impedance is [ ]
A) $-h_{fe}$ B) $A_i R_L / h_{ie}$ C) h_{ie} D) infinity

24. In simplified hybrid model of CE, the output impedance is [ ]
A) $-h_{fe}$ B) $A_i R_L / h_{ie}$ C) h_{ie} D) infinity

25. In simplified hybrid model of CB, the current gain is [ ]
A) $h_{fe} / (1 + h_{fe})$ B) $h_{fe} R_L / h_{ie}$ C) $h_{ie} / (1 + h_{fe})$ D) infinity

26. In simplified hybrid model of CB, the voltage gain is [ ]
A) $h_{fe} / (1 + h_{fe})$ B) $h_{fe} R_L / h_{ie}$ C) $h_{ie} / (1 + h_{fe})$ D) infinity

27. In simplified hybrid model of CB, the input impedance is [ ]
A) $h_{fe} / (1 + h_{fe})$ B) $h_{fe} R_L / h_{ie}$ C) $h_{ie} / (1 + h_{fe})$ D) infinity

28. In simplified hybrid model of CB, the output impedance is [ ]
A) $h_{fe} / (1 + h_{fe})$ B) $h_{fe} R_L / h_{ie}$ C) $h_{ie} / (1 + h_{fe})$ D) infinity

29. In simplified hybrid model of CC, the current gain is [ ]
A) $1 + h_{fe}$ B) 1 C) $h_{ie} + [(1 + h_{fe}) R_L]$ D) $(R_s + h_{ie}) / (1 + h_{fe})$

30. In simplified hybrid model of CC, the voltage gain is [ ]
A) $1 + h_{fe}$ B) 1 C) $h_{ie} + [(1 + h_{fe}) R_L]$ D) $(R_s + h_{ie}) / (1 + h_{fe})$

31. In simplified hybrid model of CC, the input impedance is [ ]
A) $1 + h_{fe}$ B) 1 C) $h_{ie} + [(1 + h_{fe}) R_L]$ D) $(R_s + h_{ie}) / (1 + h_{fe})$

32. In simplified hybrid model of CC, the output impedance is [ ]
A) $1 + h_{fe}$ B) 1 C) $h_{ie} + [(1 + h_{fe}) R_L]$ D) $(R_s + h_{ie}) / (1 + h_{fe})$

33. The condition for approximate analysis is [ ]
A) $R_L = R_S$ B) $h_{oe}R_L < 0.1$ C) $h_{ie} < 0.01$ D) $h_{fe} = 0$

34. If the emitter resistance in a common emitter voltage amplifier is not bypassed, it will **[GATE 2014]** [ ]
A) reduce both the voltage gain and the input impedance
B) reduce the voltage gain and increase the input impedance
C) increase the voltage gain and reduce the input impedance
D) increase both the voltage gain and the input impedance

35. For simplified CE hybrid model, if $h_{fe} = 60$, $h_{ie} = 500\Omega$ at $I_c = 3mA$, the input impedance is [ ]
A) 300Ω B) $5.1k\Omega$ C) 60Ω D) 500Ω

36. For simplified CE hybrid model, if $h_{fe} = 60$, $h_{ie} = 500\Omega$ at $I_c = 3mA$, the output impedance is [ ]
A) 660Ω B) 45Ω C) $5.1k\Omega$ D) $6.2M\Omega$

37. For simplified CE hybrid model, if $h_{fe} = 60$, $h_{ie} = 500\Omega$ at $I_c = 3mA$, the voltage gain is [ ]
A) -544 B) -612 C) 455 D) 750

38. For simplified CE hybrid model, if $h_{fe} = 60$, $h_{ie} = 500\Omega$ at $I_c = 3mA$, the current gain is [ ]
A) -60 B) 88 C) -100 D) 1

39. In the h parameter model the input and output sections are modeled as **[GATE 2000]** [ ]
A) voltage sources B) current sources
C) input section as voltage source and output section as current source
D) input section as current source and output section as voltage source

40. h-parameters are used for the low frequency analysis of BJT amplifier analysis because [ ]
A) h parameters are real numbers up to radio frequencies
B) they are easy to measure
C) readily supplied by manufacturers
D) all of the above

UNIT V
FIELD EFFECT TRANSISTOR

1. The JFET is [ ]
   A) a bipolar device B) unipolar device C) voltage controlled device D) both (B) and (C)
2. The channel of a JFET exists between [ ]
   A) gate and source B) drain and source C) gate and drain D) None of the above
3. For low values of V_{DS}, the JFET behaves like a [ ]
   A) resistance B) constant voltage device C) constant current device D) None
4. In an N channel JFET **[RRB-JE-2012]** [ ]
   A) the current carriers are holes B) the current carriers are electrons
   C) V_{GS} is positive D) the input resistance is very low
5. In a P channel JFET [ ]
   A) the current carriers are electrons B) the current carriers are holes
   C) V_{GS} is negative D) the input resistance is very small
6. For an N channel JFET **(GATE 1990)** [ ]
   A) V_{GS} can vary between zero negatively to V_{GSO} B) V_{GS} can vary between zero positively to V_{GSO}
   C) pinch off occurs for positive V_{GS} D) V_{DD} is negative
7. An FET cannot operate at $V_{GS} = 0V$. The FET is [ ]
   A) JFET B) D-MOSFET C) E-MOSFET D) None of the above
8. The transconductance g_m of JFET is defined as [ ]
   A) I_D / V_{GS} B) I_D / V_{DS} C) V_{GS} / I_D D) I_{DSS} / I_D
9. The amplification factor μ of JFET is given by **[IES-2010]** [ ]
   A) $\mu=g_m/r_d$ B) $g_m = \mu * r_d$ C) $\mu=g_m*r_d$ D) $r_d =g_m- \mu$
10. The drain resistance r_d is given by [ ]
    A) $\mu * g_m$ B) I_D / V_{DS} C) V_{DS} / I_D D) none of the above
11. Ideally, the equivalent circuit of an FET consists of **[GATE 2017]** [ ]
    A) a resistance between drain and source
    B) a current source between the gate and the source
    C) a current source between the drain and the source
    D) none of the above
12. The magnitude of the current source in the ac equivalent circuit of an FET depends on [ ]
    A) the dc supply voltage B) V_{DS} C) externally drain resistance C) none of the above
13. Which one of the following has the highest input resistance? [ ]
    A) NPN transistor in CB configuration B) PNP transistor in CE configuration
    C) N type channel JFET D) P type channel MOSFET
14. The current conduction of JFET involved [ ]
    A) a flow of minority carriers B) a flow of majority carriers
    C) Recombination D) none of the above
15. The JFET is also called as [ ]
    A) voltage controlled device B) current controlled device C) bipolar device D) none
16. Which of the following statements is true? **[GATE 2014]** [ ]
    A) FET and BJT, both are unipolar B) FET and BJT, both are bipolar
    C) FET is bipolar and BJT is unipolar D) FET is unipolar and BJT is bipolar
17. An FET has a [ ]
    A) very high input resistance B) very low input resistance
    C) high connection emitter junction D) none of the above
18. For small values of drain to source voltage, JFET behaves like a [ ]
    A) resistor B) constant current source C) constant voltage source D) none of the above
19. In a JFET, the primary control on drain current is exerted by [ ]
    A) channel resistance B) size of depletion regions C) gate reverse bias D) none of the above
20. After V_{DS} reaches pinch off voltage V_P in a JFET, the drain current becomes [ ]
    A) zero B) saturated C) low D) none of the above
21. The Drain Characteristics curve of a JFET is a graph of: [ ]
    A) I_S versus V_{DS} B) I_C versus V_{CE} C) I_D versus V_{DS} D) I_D versus V_{GS}
22. In a JFET, drain current is maximum when V_{GS} is **[GATE 2006]** [ ]
    A) zero B) negative C) positive D) none of the above

23. A JFET has _____ input impedance when compared to BJT. [ ]
A) low B) high C) zero D) none of the above
24. The drain to source voltage at which the drain current becomes nearly constant is called [ ]
A) barrier voltage B) breakdown voltage C) high voltage D) pinchoff voltage
25. The Transfer Characteristics curve of a JFET is a graph of: [ ]
A) I_S versus V_{DS} B) I_C versus V_{CE} C) I_D versus V_{DS} D) I_D versus V_{GS}
26. The depletion MOSFET differs from a JFET in the sense that it has no [ ]
A) channel B) gate C) PN junctions D) substrate
27. For the operation of enhancement n-channel MOSFET, the gate voltage will be **[IES 2014]** [ ]
A) high positive B) high negative C) low positive D) zero
28. The gate terminal of JFET corresponds to _____ terminal of BJT. [ ]
A) collector B) base C) emitter D) none of the above
29. The main factor which differentiates depletion MOSFET from an enhancement only MOSFET is the absence of **[GATE 2009]** [ ]
A) insulated gate B) electrons C) channel D) PN Junction
30. The phase shift between input and output of common source amplifier is [ ]
A) 0^0 B) 180^0 C) 90^0 D) none of the above
31. In a FET amplifier, the source follower is [ ]
A) CS amplifier B) CG amplifier C) CD amplifier D) none of the above
32. The voltage controls the drain current flow in FET is [ ]
A) V_{GS} B) V_{DS} C) V_{CC} D) none of the above
33. The gate source voltage of a JFET should be **[GATE 2008]** [ ]
A) forward biased B) reverse biased C) unbiased D) none of the above
34. The input impedance of an ideal JFET is [ ]
A) impossible to predict B) approaches to unity C) approaches to infinity D) none of the above
35. The charge carriers in an N channel JFET are [ ]
A) electrons B) holes C) neutrons D) none of the above
36. The saturation region of JFET is also known as [ ]
A) Pinch off B) analog C source D) Ohmic
37. A JFET can operate in [ ]
A) only depletion mode B) only enhancement mode C) both depletion and enhancement D) none
38. When a JFET is pinched off, the depletion layers are [ ]
A) conducting B) close together C) Far apart D) none of the above
39. The Insulated Gate Field Effect Transistor is **[GATE 2009]** [ ]
A) MOSFET B) JFET C) BJT D) none of the above
40. When a JFET is cut off, its like a _____ switch and when its saturated its like _____ switch. [ ]
A) closed, closed B) open, closed C) open, open D) none of the above

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